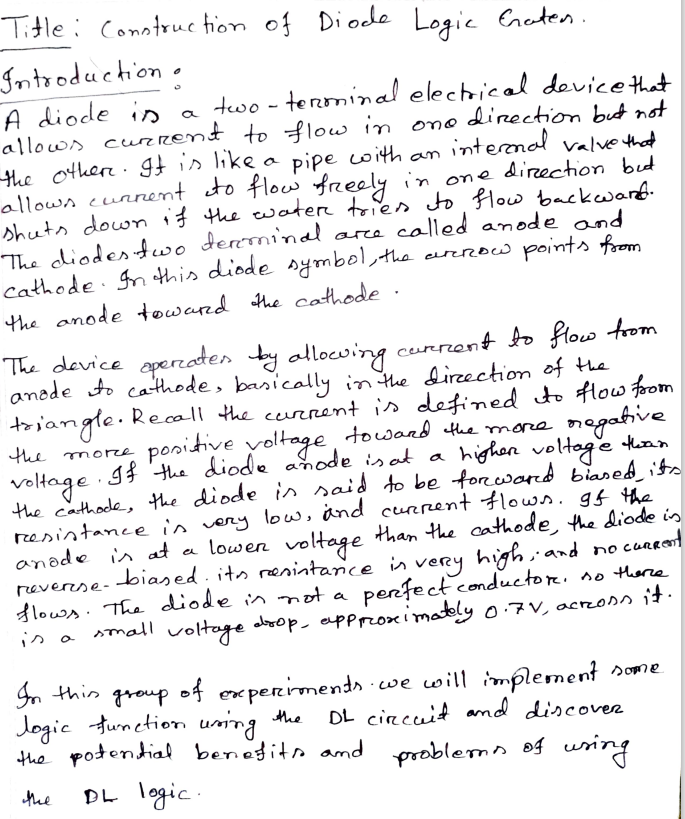
**Experiment Number-1**

Submitted by: Name: MD SAIFUL ISLAM ID: 18-36363-1 Course: Digital Electronic



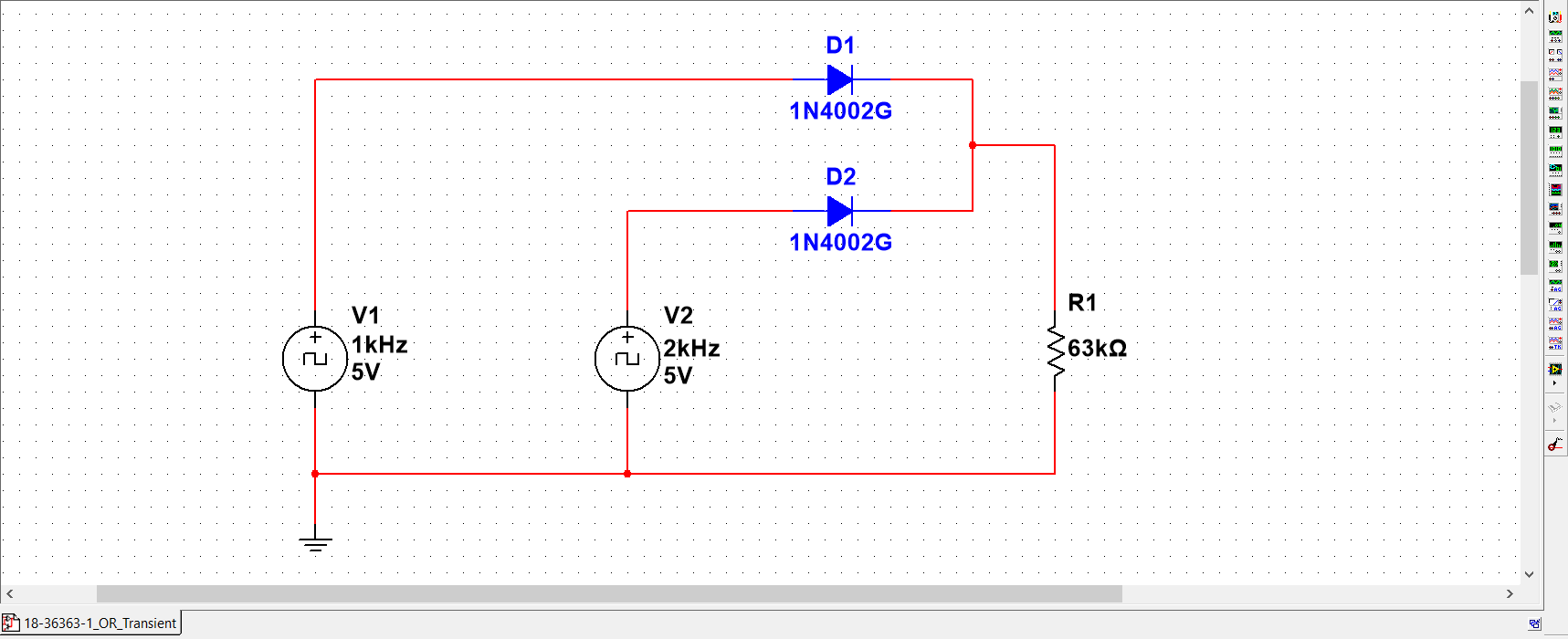
**Block Diagram:**

Figure 1: DL-OR Gate

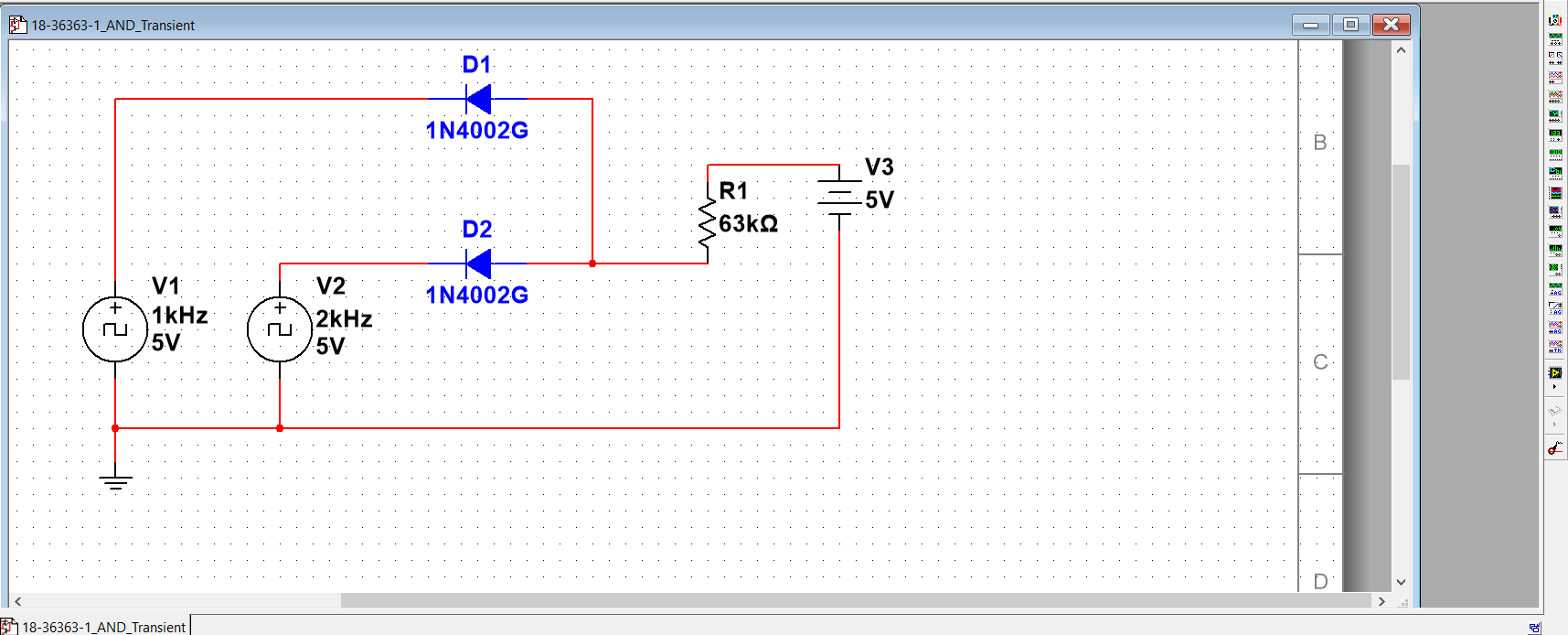


Figure 2: DL-AND Gate

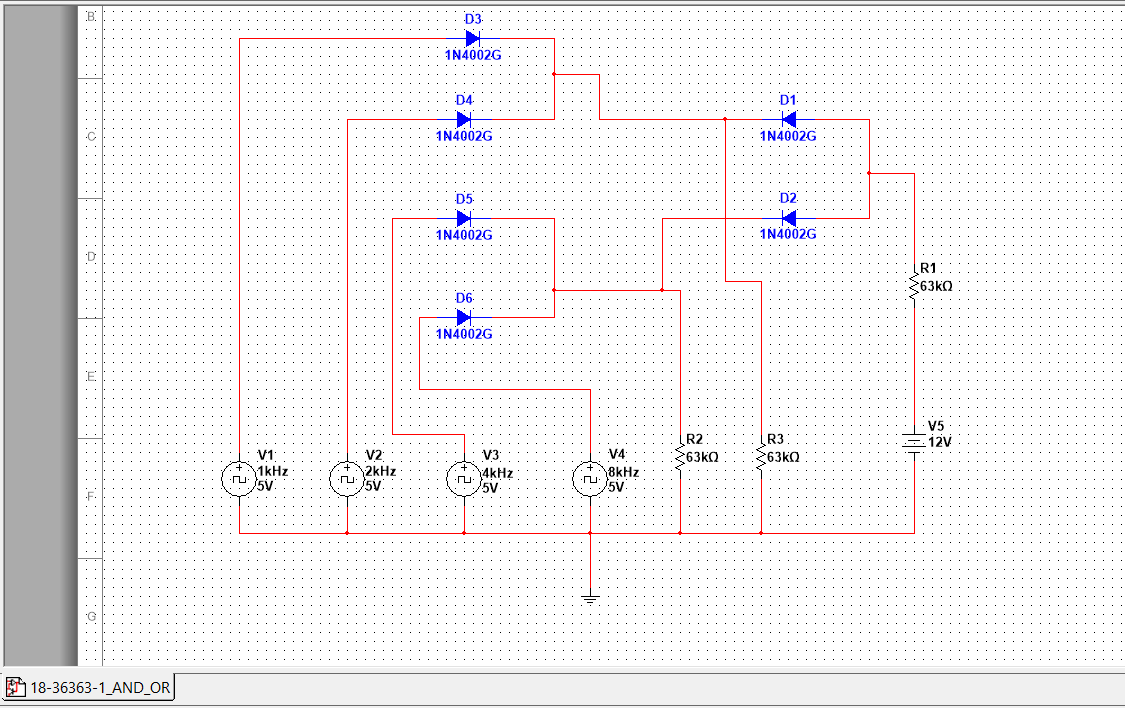
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Figure 3: DL-AND-OR Gate

**Graph:**

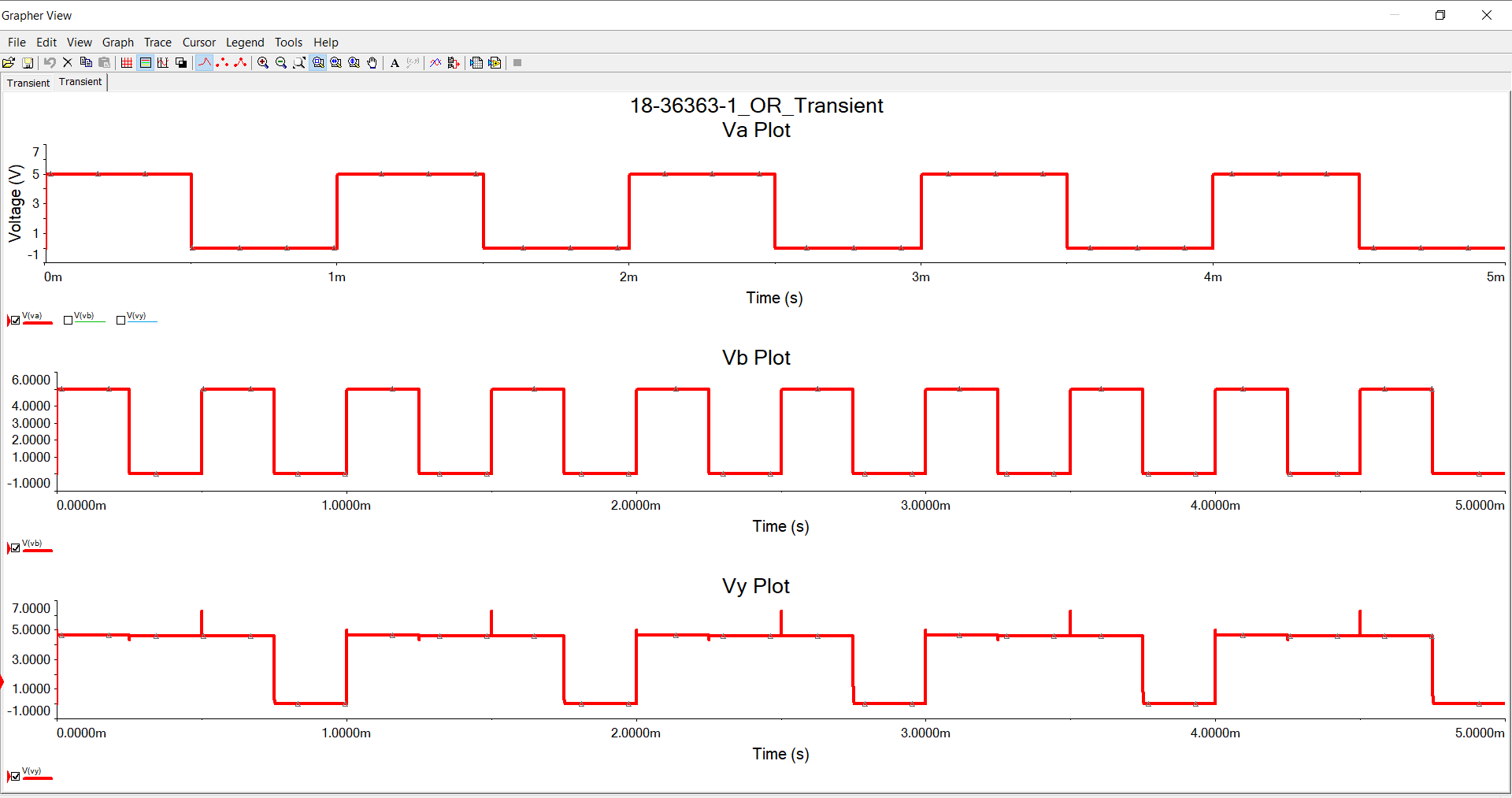
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Figure 4: DL-OR Gate Graph

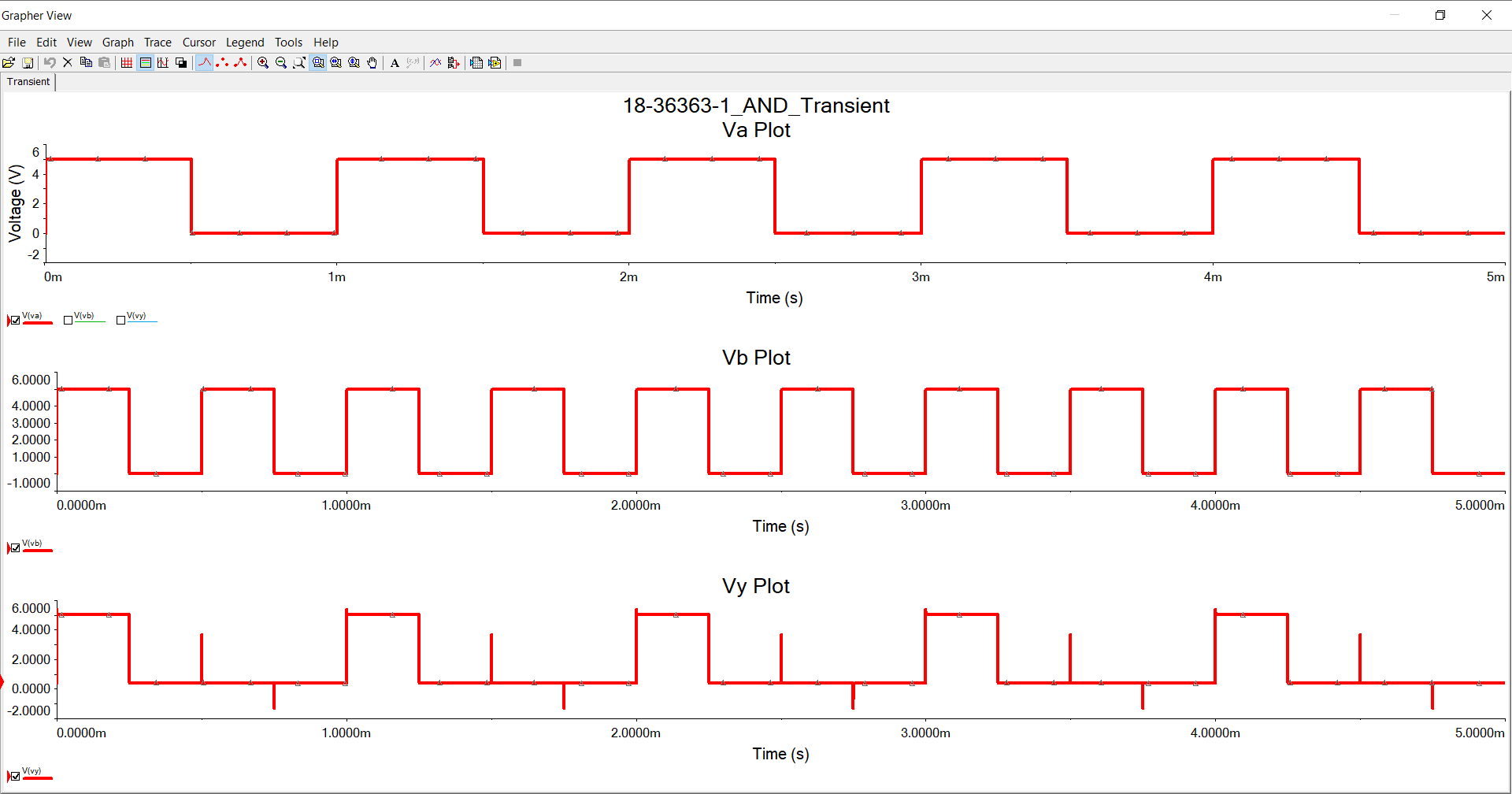
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Figure 5: DL-AND Gate Graph

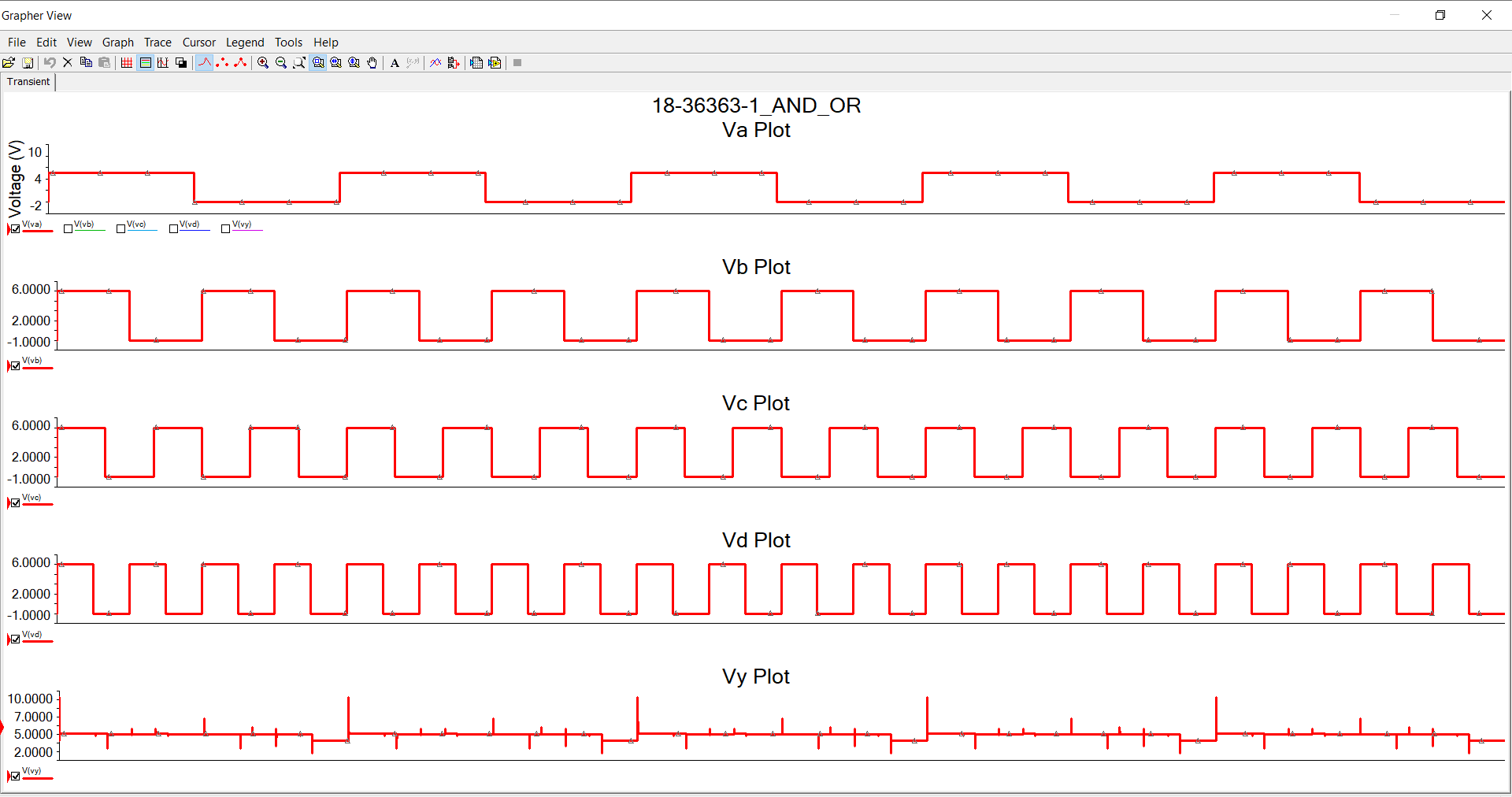
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Figure 6: DL-AND-OR Gate Graph

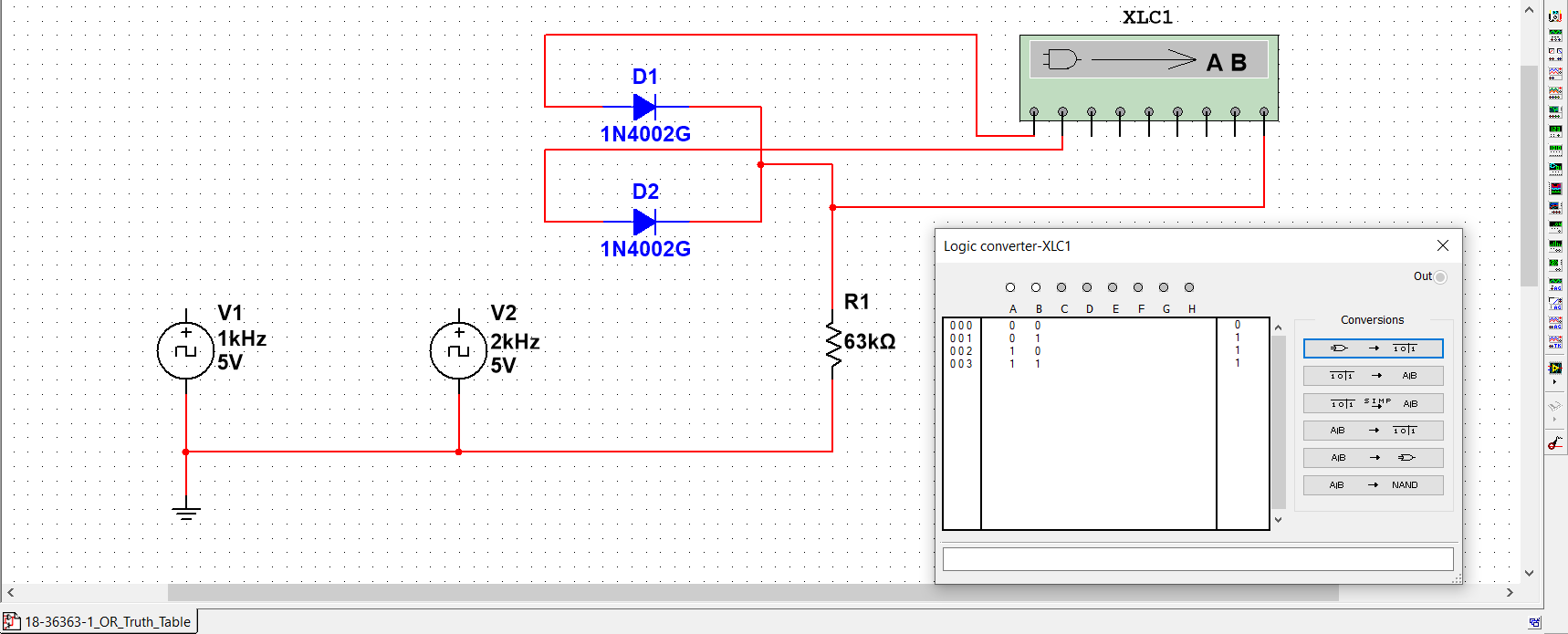
**TruthTable:**

Figure 7: DL-OR Gate Truth Table.

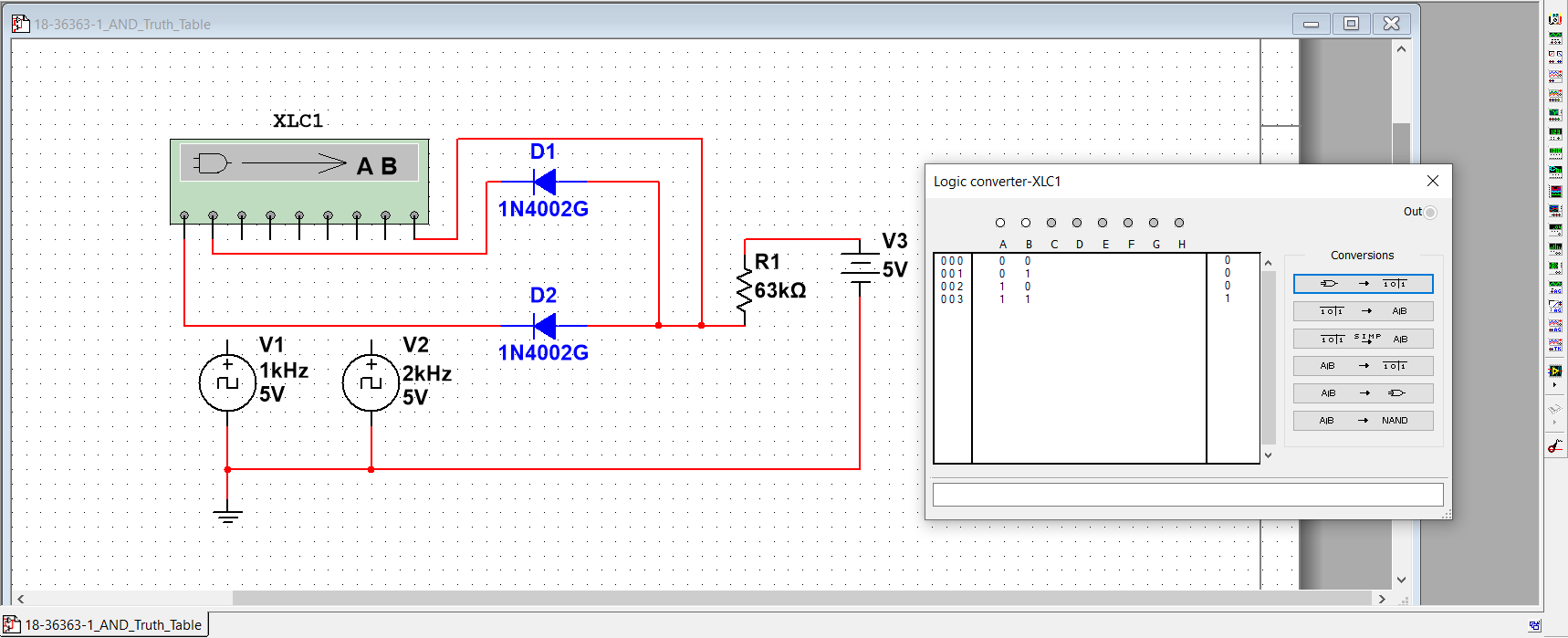
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Figure 8: DL-AND Gate Truth Table.

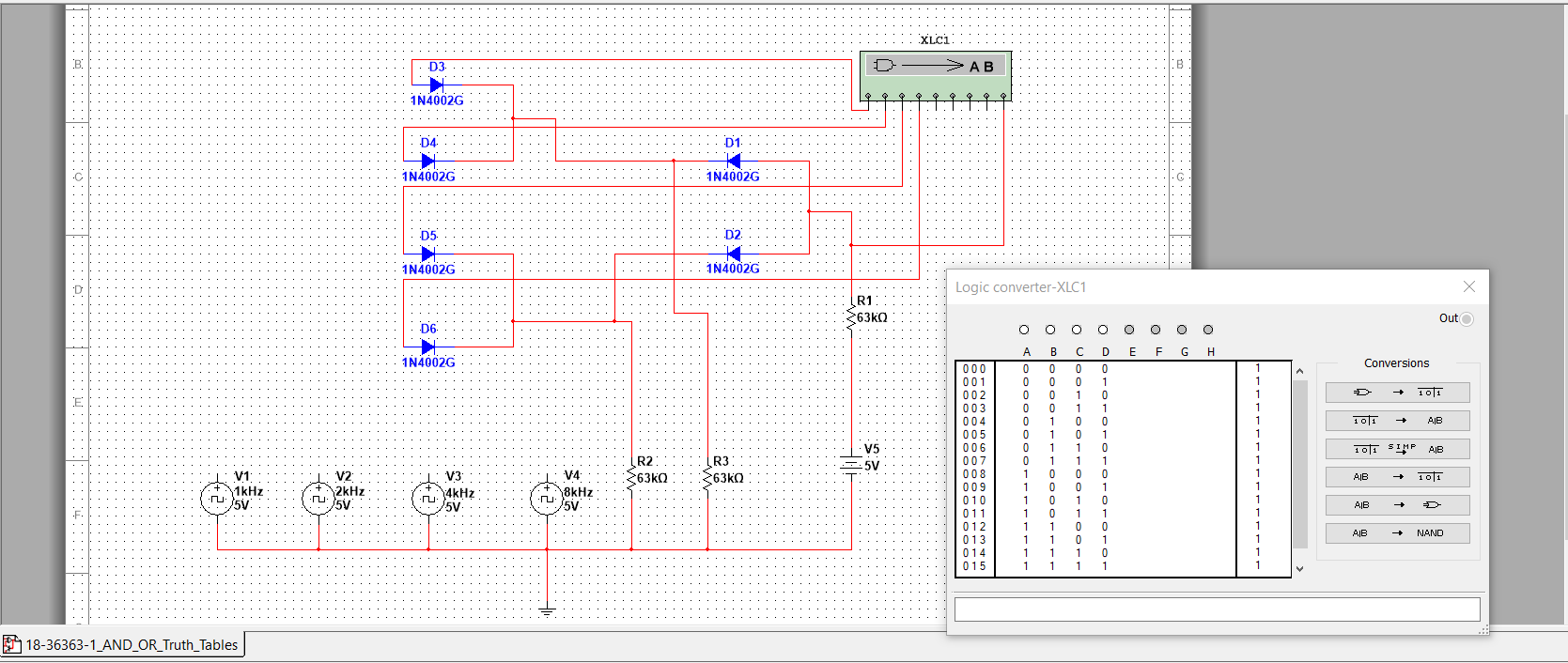
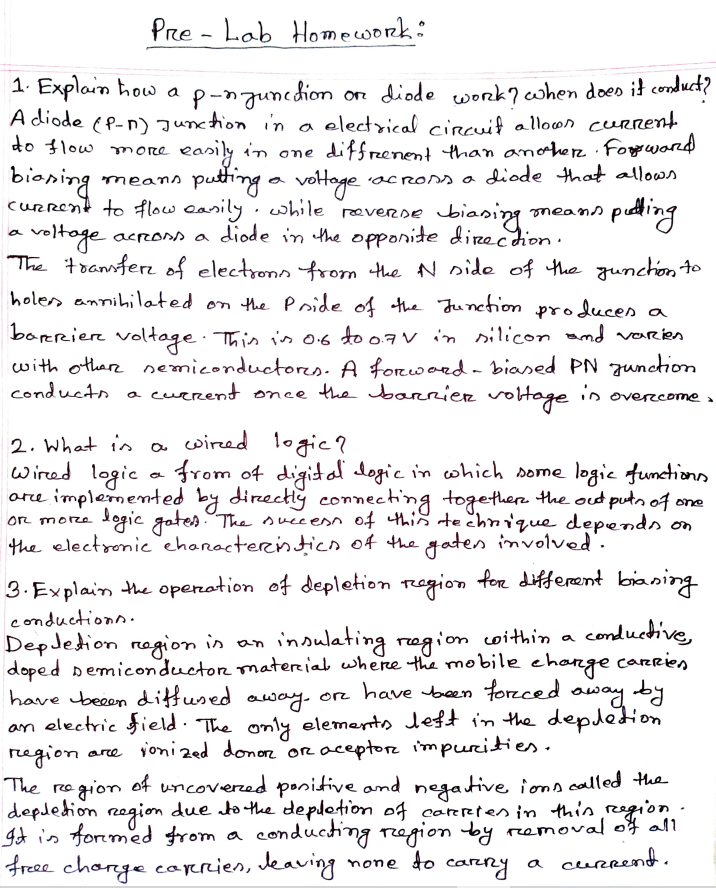
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Figure 9: DL-AND-OR Gate Graph

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